16-BIT, HIGH-SPEED, LOW-NOISE, VOLTAGE OUTPUT, DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **16-Bit Monotonic**
- **±5-V Rail-to-Rail Output**
- **Fast Settling: 0.65 μs**
- **Fast Slew Rate: 35 V/μs**
- **Low Noise: 20 nV/√Hz**
- **Low Glitch Energy: 0.5 nV-s**
- **Low Power-On Transient**
- **On-Chip Digital Low-Pass Filter**
- **Programmable Oversampling**
- **16-MSPS Update Rate (Filter On)**
- **30-MHz Serial Interface**
- **1.8-V to 5.5-V Logic Compatible**
- **TSSOP-16 Package**

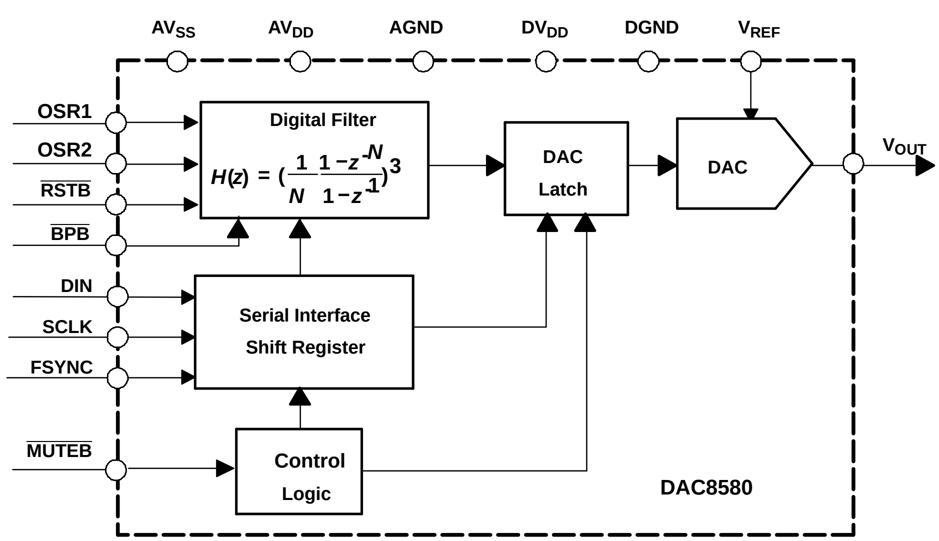
APPLICATIONS

- **Waveform Generation**
- **CRT Projection TV Digital Convergence**
- **Automated Test Equipment**
- **Industrial Process Control**
- **Music Synthesis**
- **Ultrasound**

DESCRIPTION

The DAC8580 is a 16-bit, high-speed, low-noise, voltage-output DAC designed for waveform generation applications. It operates from dual ±5-V power supplies and requires only a single external reference. The DAC8580 is capable of generating output signal frequencies up to 1 MHz. The DAC8580 significantly relaxes, or removes, the need for external de-glitchers, analog filters and high-swing output buffers. It incorporates a programmable digital interpolation filter capable of oversampling the input word rate by 2, 4, 8, or 16. The digital filter can be bypassed on-the-fly, or can be permanently turned off. The fast 30-MHz serial interface is compatible with right-justified digital audio format. The DAC8580 is specified from –40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM OF DAC8580



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. This device is rated at 1500 V HBM and 1000 V CDM.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC8580	16-TSSOP	PW	–40°C TO +85°C	D8580I	DAC8580IPW	90-Piece Tube
					DAC8580IPWR	2000-Piece Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

AV_{DD} or DV_{DD} to AV_{SS}		–0.3 V to 12 V
Digital input voltage to AV_{SS}		–0.3 V to 12 V
V_{OUT} or V_{REF} to AV_{SS}		–0.3 V to 12 V
DGND and AGND to AV_{SS}		–0.3 V to 6 V
Operating temperature range		– 40°C to +85°C
Storage temperature range		– 65°C to +150°C
Junction temperature range (T_J max)		+150°C
Power dissipation:	Thermal impedance (Θ_{JA})	118°C/W
	Thermal impedance (Θ_{JC})	29°C/W
Lead temperature, soldering:	Vapor phase (60 s)	215°C
	Infrared (15 s)	220°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $+AV_{DD} = +5$ V, $–AV_{DD} = –5$ V, $DV_{DD} = +5$ V, $V_{REF} = 4.096$ V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
Resolution		16			Bits
Linearity error			±0.05		% FSR
Differential linearity error			±0.25	±1	LSB
Gain error		1	2	3	% FSR
Gain drift			±3		ppm/°C
Bipolar zero error	V_{REF} = 4.096 V		±5	±25	mV
Bipolar zero drift	From –40°C to +85°C		±20		µV/°C
Total drift	From –40°C to +85°C		±8		ppm/°C
OUTPUT CHARACTERISTICS					
Voltage output range	AV_{DD} = 6 V, AV_{SS} = –6 V, V_{REF} = 5.5 V	–5.5		5.5	V
Maximum current drive capability	At full speed, driving resistive load (1)		±25		mA
Output Impedance			18		Ω

(1) Sourcing and sinking dc currents larger than 25 mA is not recommended.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $+AV_{DD} = +5$ V, $–AV_{DD} = –5$ V, $DV_{DD} = +5$ V, $V_{REF} = 4.096$ V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Settling time (large signal)	C_L <200 pF, R_L = 2 kΩ, to 0.1% FS, 8-V step		0.35	0.65	µs
	To 0.003% FS, 8-V step		1.0		
Settling time (small signal)	To 0.003% FS, 100-mV step		0.15		µs
Slew rate	From 10% to 90% of % FSR		35		V/µs
Code-to-code glitch impulse	1 LSB change around major carry		5		mV
Code-to-code glitch energy	1 LSB change around major carry		0.5		nV-s
Overshoot	Limited by slew-boost circuit operation during large-signal swings.		100		mV
Digital feedthrough (2)	SCLK toggling		0.5		nV-s
Voltage output noise	Frequency = 100 kHz		20		nV/√Hz
	Frequency = 10 kHz		25		nV/√Hz
	F = 0.1 Hz to 10 Hz		25		µVp-p
Power supply rejection	V_{DD} varies ±10%		0.3		mV/V
REFERENCE INPUT CHARACTERISTICS					
Reference input voltage range		3.0		AV_{DD}	V
Reference input impedance			5		kΩ
Reference input capacitance			5		pF
Reference multiplying bandwidth	Large signal (1 V peak-to-peak)		3		MHz
Reference multiplying bandwidth	Small signal		10		MHz
AC CHARACTERISTICS					
2nd Harmonic distortion	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Digital filter is OFF		–72		dB
	DAC output signal (sine wave) frequency = 40 kHz, DAC input update rate = 1 MSPS, Digital filter oversampling rate = 16 (3)		–72	–56	
	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS Software calibrated, digital filter is OFF (4)		–100		
3rd Harmonic distortion	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Digital filter is OFF		–72		dB
	DAC output signal (sine wave) frequency = 40 kHz, DAC input update rate= 1 MSPS, Digital filter oversampling rate = 16 (3)		–72	–56	
	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Software calibrated, digital filter is OFF (4)		–100		
Spurious free dynamic range (SFDR)	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Digital filter is OFF		72		dB
	DAC output signal (sine wave) frequency = 40 kHz, DAC input update rate= 1 MSPS, Digital filter oversampling rate =16 (3)	56	70		dB
	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Software calibrated, digital filter is OFF (4)		–100		

(2) Digital feedthrough error is defined as the area of the impulse injected into the analog output from the digital input, during the toggling of the digital input.
(3) No analog filter is used. On-chip digital filter is set at oversampling ratio of 16. High-speed digitizer has 10-MHz input bandwidth. This specification is 100% tested during production.
(4) Software calibration requires the user to calibrate the linearity error using a precision digitizer and provide the DAC inputs from a lookup table.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $+AV_{DD}$ = +5 V, $–AV_{DD}$ = –5 V, DV_{DD} = +5 V, V_{REF} = 4.096 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion (THD)	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Digital filter is OFF		–70		dB
	DAC output signal (sine wave) frequency = 40 kHz, DAC input update rate =1 MSPS, Digital filter oversampling rate =16 (3)		–68	–56	
	DAC output signal (sine wave) frequency = 1 kHz, DAC input update rate = 192 KSPS, Software calibrated, digital filter is OFF (4)		–98		
Signal to noise ratio (SNR)	DAC output signal is 1-kHz sine wave, –1 dBFS. Noise bandwidth is from 0 to 10 kHz. (5)		110		dBFS
Maximum output frequency (without external analog filter)	Serial clock = 16 MHz, Digital filter oversampling rate =16 THD > 50 dBs, without analog filter		0.2		MHz
Maximum output frequency (with external analog filter)	Serial clock = 32 MHz, Digital filter oversampling rate = 8 (6) THD > 50 dBs, with analog filter		1		MHz
Maximum output update rate				16	MHz
DIGITAL INPUT CHARACTERISTICS					
V_{IH}		0.7 x DV_{DD}		DV_{DD}	V
V_{IL}		GND		0.3 x DV_{DD}	V
Input leakage current			±0.05	±1	µA
Input capacitance				5	pF
Power-on delay	From V_{DD} high to $\overline{CS}$ low		130		µs
POWER SUPPLY CHARACTERISTICS					
$+AV_{DD}$		4.0	5	6.0	V
$–AV_{DD}$		–6.0	–5	–4.0	V
DV_{DD}		1.8		AV_{DD}	V
I_{DD}	AV_{DD} = 5.0 V, AV_{SS} = –5.0 V, V_{REF} = 4.096 V, I_{REF} included		17	24	mA
I_{SS}			–23	–32	mA
TEMPERATURE RANGE					
Specified performance		–40		85	°C

(5) A precision delta-sigma digitizer is used to make the measurement.
(6) An oversampling ratio of 16X cannot be supported at 32 MHz clock frequency. 8X oversampling can be used instead to generate a 1-MHz output. To generate output frequencies over 200 kHz, use of analog anti-imaging filters are highly recommended. The DAC8580 digital filter still relaxes the analog filter requirements. At F_{OUT} >200 kHz, large-signal waveforms have overshoot/undershoot due to the settling characteristics of the output amplifiers. Small-signal waveforms don't show this behavior.

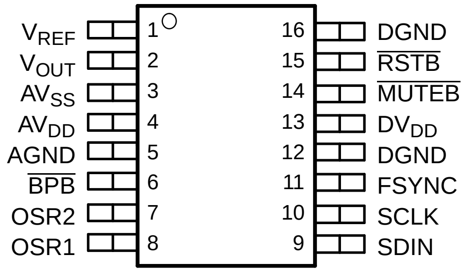
TIMING CHARACTERISTICS

At –40°C to 85°C, DV_{DD} = +5 V, $+AV_{DD}$ = +5 V, $–AV_{DD}$ = –5 V, unless otherwise noted (1) (2)

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	33		ns
t_{wsck}	SCLK high or low time	16		ns
t_{su}	Data setup time (input)	5		ns
t_{hi}	Data hold time (input)	5		ns
t_{SWF}	FSYNC setup time	5		ns
t_{HWF}	FSYNC hold time	5		ns
t_r	Rise time	20	1	ns
t_f	Fall time	20	1	ns
$t_{WFUPDAC}$	Delay from falling edge of $\overline{FSYNC}$ to loading DAC latch (3)	1.5		t_{sck}

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.
(3) OUTPUT of pin V_{OUT} changes to new level immediately (within settling time) after DAC register is loaded.

TSSOP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	V_{REF}	Reference input voltage; 3 V to AV_{DD}.
2	V_{OUT}	DAC output voltage; output swing is $\pm V_{REF}$
3	AV_{SS}	Negative analog supply voltage; tie to –5 V
4	AV_{DD}	Positive analog supply voltage; tie to +5 V
5	AGND	Ground reference for analog circuitry of the device
6	$\overline{\text{BPB}}$	Active-low, asynchronous digital input for filter bypass
7	OSR2	Digital input for selecting the oversampling ratio
8	OSR1	Digital input for selecting the oversampling ratio
9	DIN	Digital input, serial data
10	SCLK	Digital input, serial bit clock
11	FSYNC	Digital input. FSYNC is word clock.
12	DGND	Ground reference for digital circuitry
13	DV_{DD}	Positive digital supply, 1.8-V to 5.5-V compatible
14	$\overline{\text{MUTEB}}$	Digital input, actime low, for forcing the output to mid-scale.
15	$\overline{\text{RSTB}}$	Filter reset. Active-low, asynchronous digital input for disabling all digital filter activity.
16	DGND	Must connect to digital ground reference to ensure correct operation.

RIGHT-JUSTIFIED AUDIO TIMING DIAGRAM

The DAC8580 serial interface timing uses a single channel (mono) version of right-justified audio format. The input data is latched into the device input shift register on the rising edge of SCLK, MSB first. The falling edge of FSYNC latches the last 16 bits of received data (right-justified) from the shift register into a temporary register, which connects to either the digital filter or the DAC latch. Data in the temporary register is transferred to the DAC latch (when digital filter is off), or to the digital filter (when the filter is on) on the second rising SCLK edge after the falling edge of FSYNC. For operating the digital filter, a continuous SCLK is required.

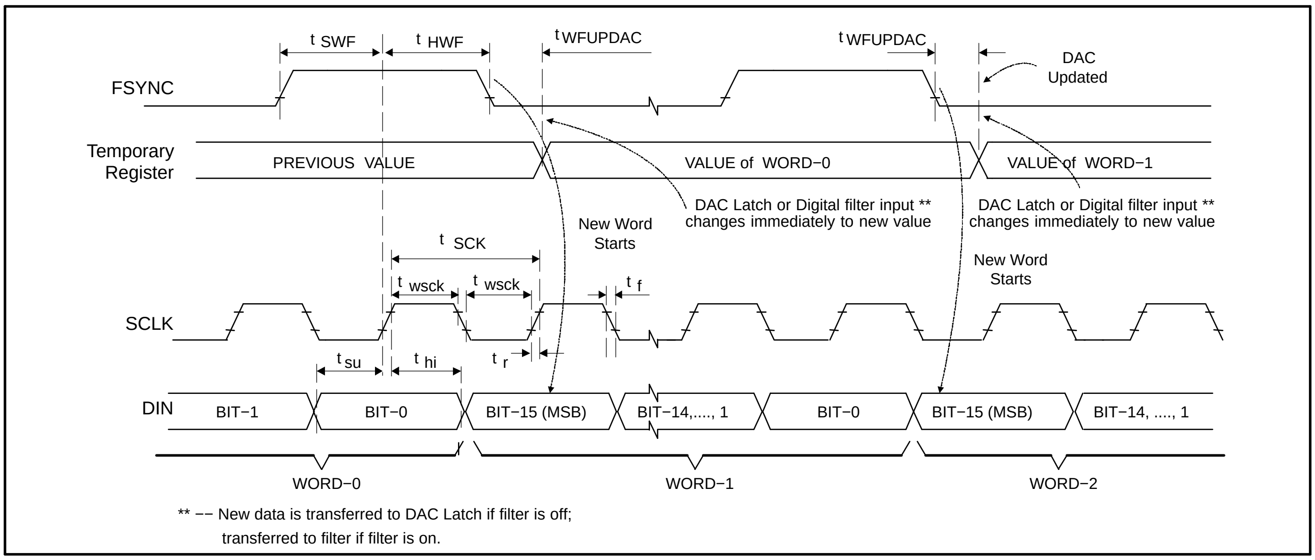


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS (AVDD = 5 V, AVSS = –5 V, VREF = 4.096 V, unless otherwise noted)

LINEARITY ERROR vs INPUT CODE

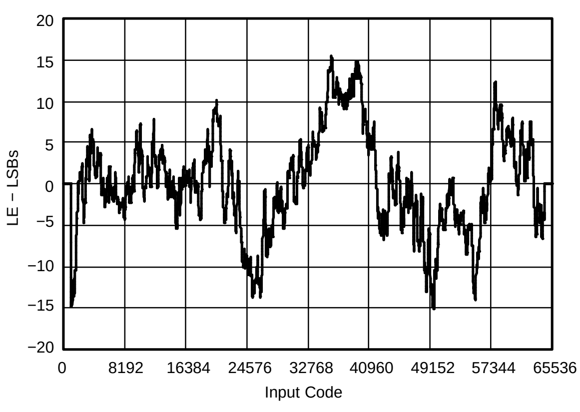


Figure 2.

DIFFERENTIAL LINEARITY ERROR vs INPUT CODE

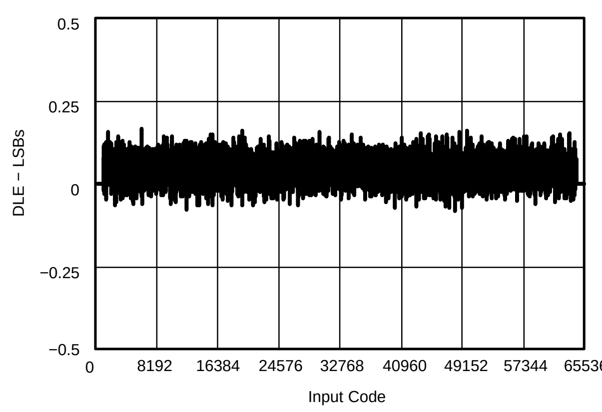


Figure 3.

TYPICAL CHARACTERISTICS (AVDD = 5 V, AVSS = –5 V, VREF = 4.096 V, unless otherwise noted) (continued)

INTEGRAL NONLINEARITY ERROR vs VREF

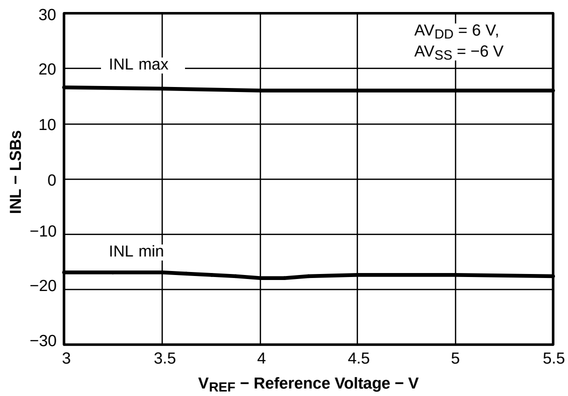


Figure 4.

INTEGRAL NONLINEARITY ERROR vs SUPPLY VOLTAGE

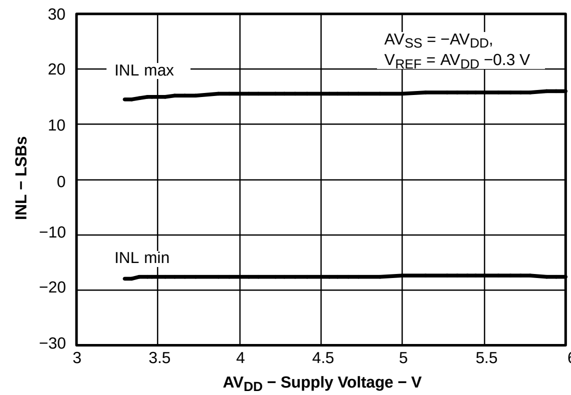


Figure 5.

OFFSET ERROR vs TEMPERATURE

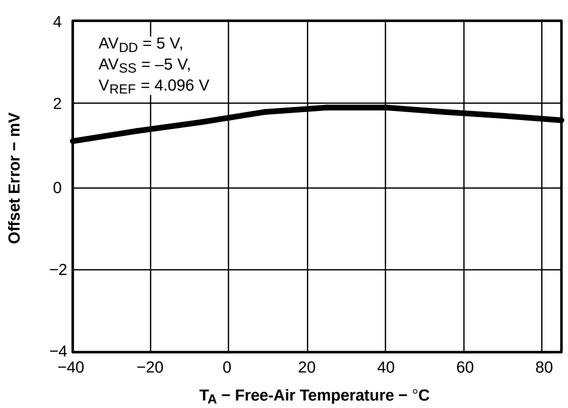


Figure 6.

GAIN ERROR vs TEMPERATURE

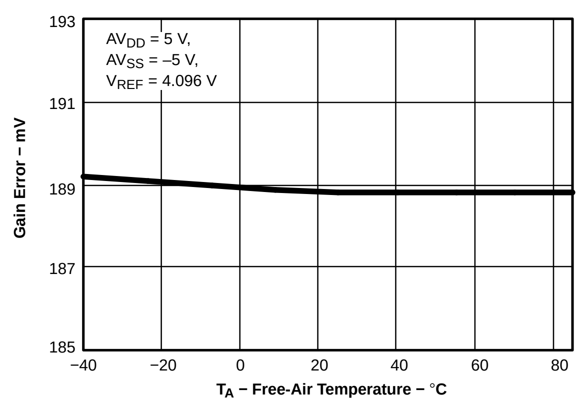


Figure 7.

POSITIVE SUPPLY CURRENT - I_{DD} vs TEMPERATURE

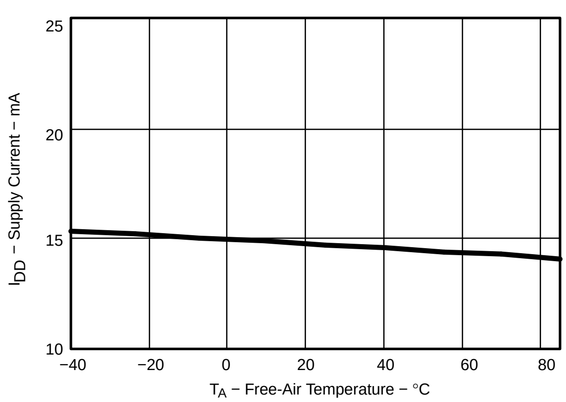


Figure 8.

NEGATIVE SUPPLY CURRENT - I_{SS} vs TEMPERATURE

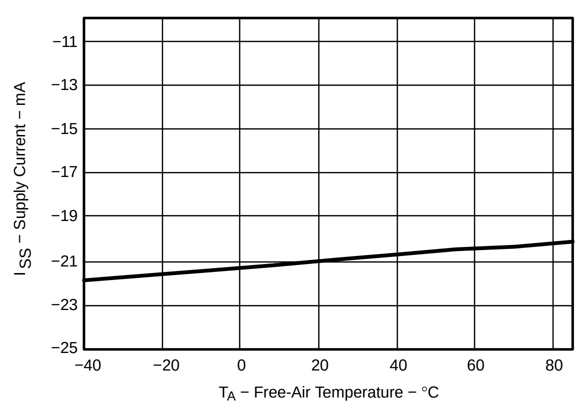


Figure 9.

TYPICAL CHARACTERISTICS (AVDD = 5 V, AVSS = –5 V, VREF = 4.096 V, unless otherwise noted) (continued)

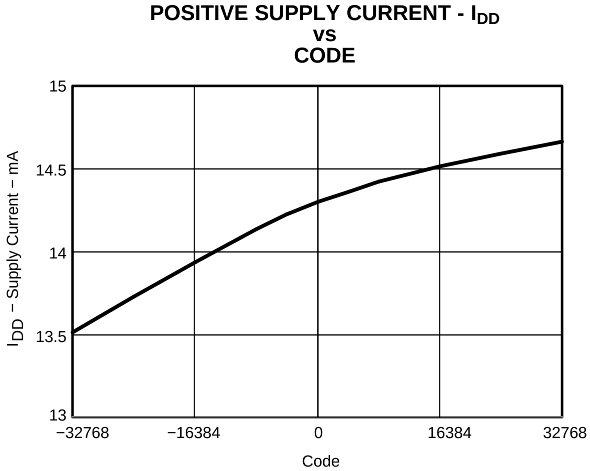


Figure 10.

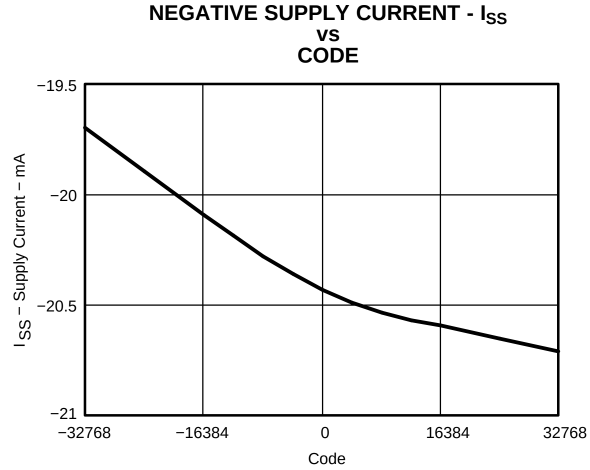


Figure 11.

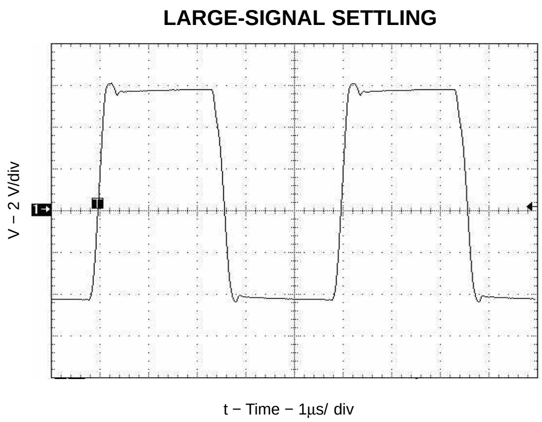


Figure 12.

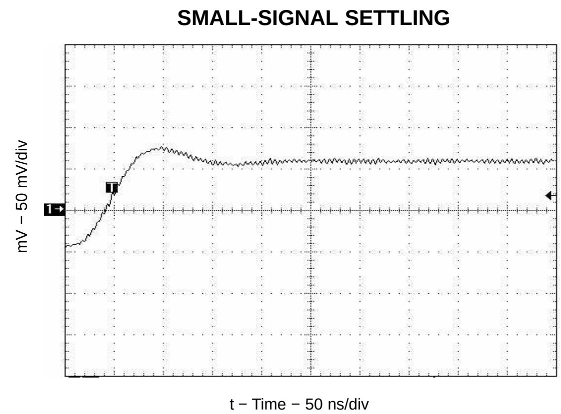


Figure 13.

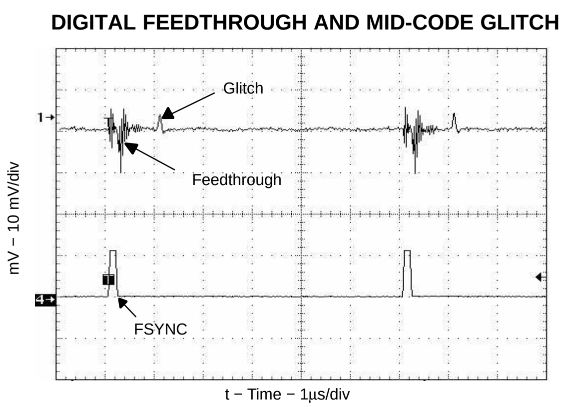


Figure 14.

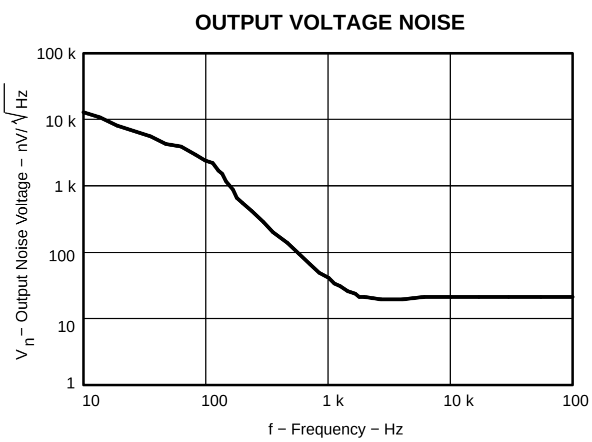


Figure 15.

TYPICAL CHARACTERISTICS (AVDD = 5 V, AVSS = –5 V, VREF = 4.096 V, unless otherwise noted) (continued)

SINE WAVE OUTPUT
Fo = 30 kHZ

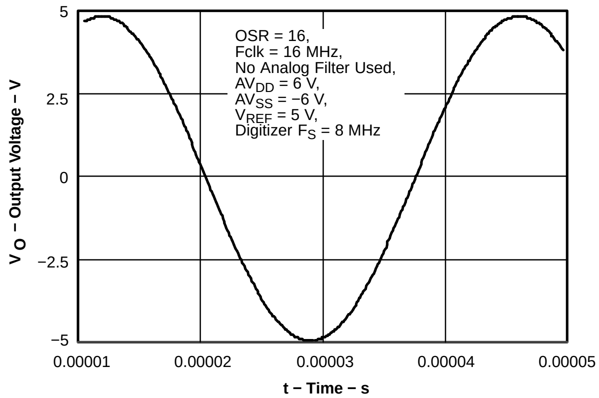


Figure 16.

POWER SPECTRAL DENSITY
Fo = 30 kHz

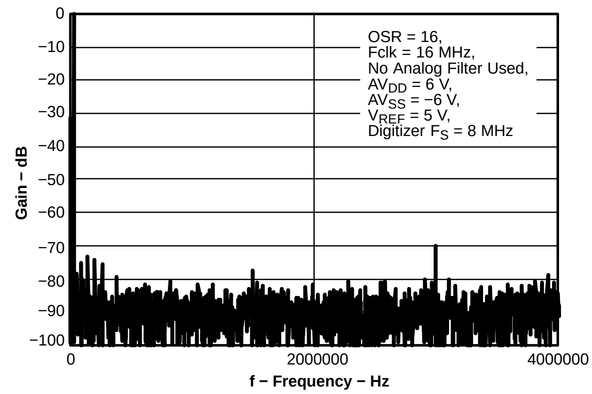


Figure 17.

SINE WAVE OUTPUT
Fo = 50 kHz

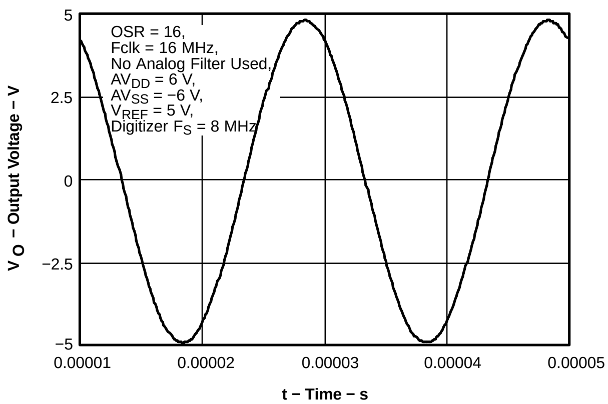


Figure 18.

POWER SPECTRAL DENSITY
Fo = 50 kHz

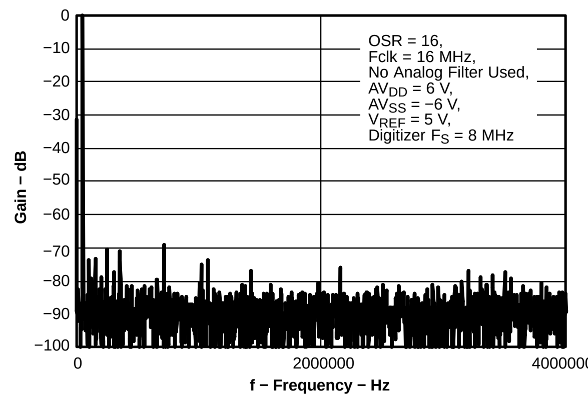


Figure 19.

SINE WAVE OUTPUT
Fo = 100 kHz

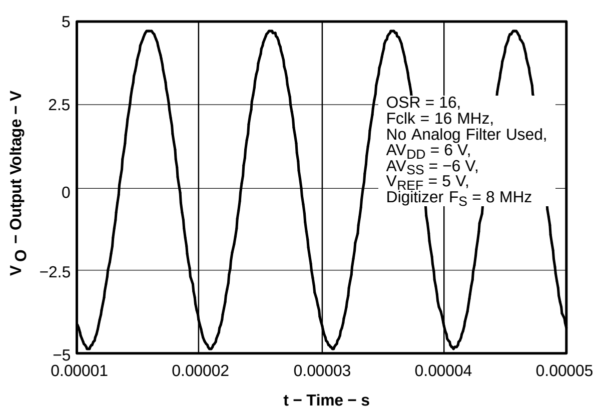


Figure 20.

POWER SPECTRAL DENSITY
Fo = 100 kHz

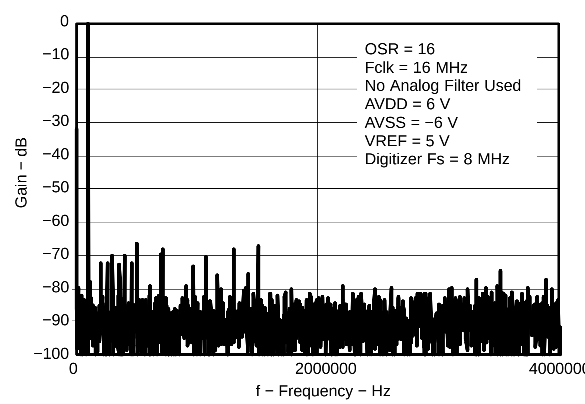


Figure 21.

TYPICAL CHARACTERISTICS (AVDD = 5 V, AVSS = –5 V, VREF = 4.096 V, unless otherwise noted) (continued)

SINE WAVE OUTPUT
Fo = 150 kHz

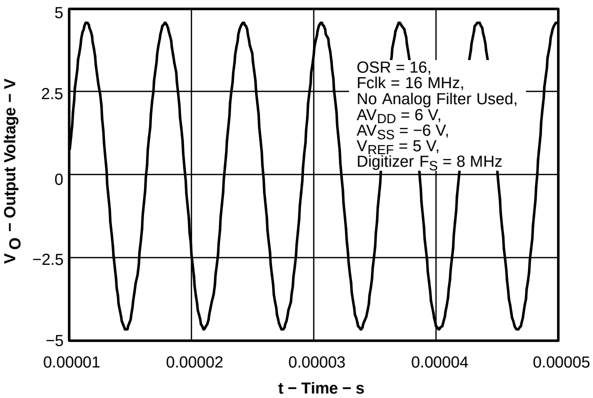


Figure 22.

POWER SPECTRAL DENSITY
Fo = 150 kHz

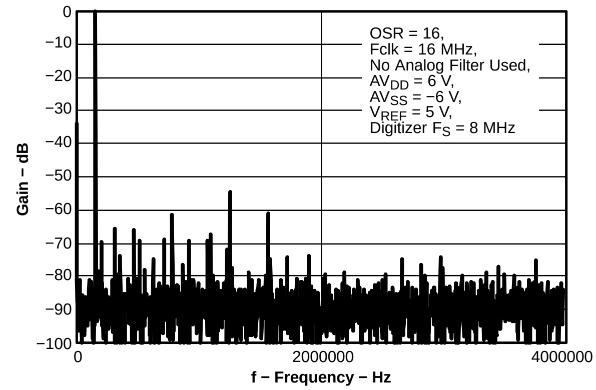


Figure 23.

SINE WAVE OUTPUT
Fo = 200 kHz

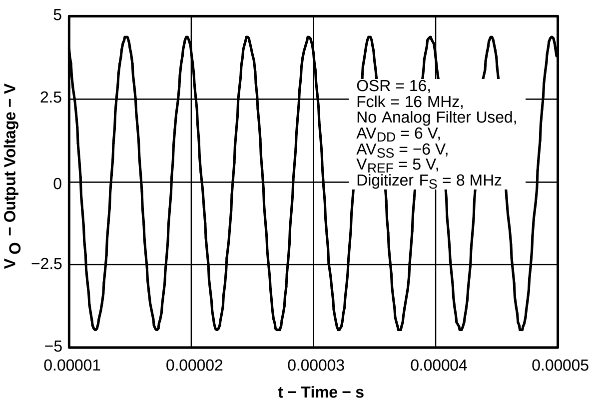


Figure 24.

POWER SPECTRAL DENSITY
Fo = 200 kHz

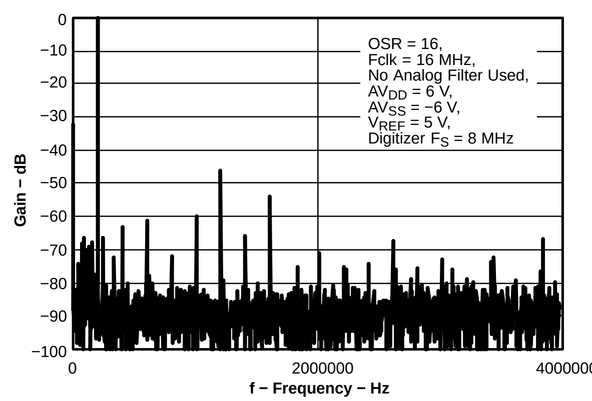


Figure 25.

POWER SPECTRAL DENSITY
FROM DC TO 6 kHz

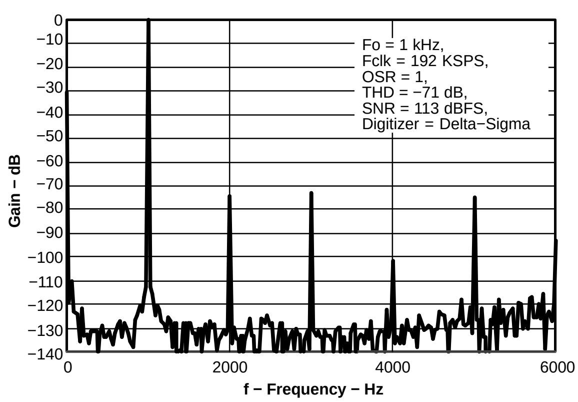


Figure 26.

TOTAL HARMONIC DISTORTION
AND SPURIOUS FREE DYNAMIC RANGE
vs
CLOCK FREQUENCY

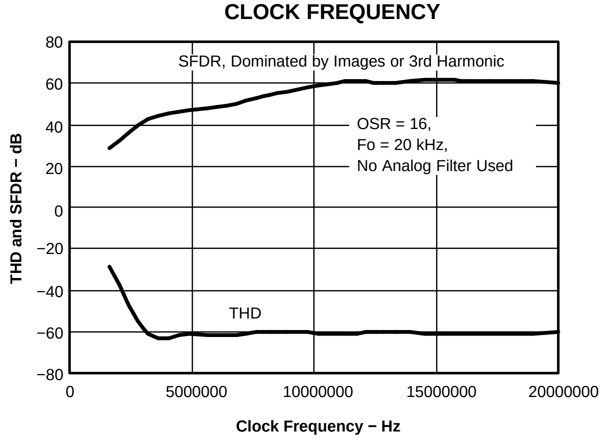


Figure 27.

TYPICAL CHARACTERISTICS (AVDD = 5 V, AVSS = –5 V, VREF = 4.096 V, unless otherwise noted) (continued)

TOTAL HARMONIC DISTORTION AND SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY

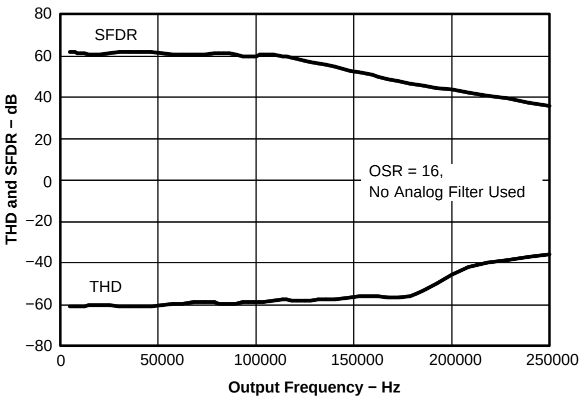


Figure 28.

TOTAL HARMONIC DISTORTION AND SPURIOUS FREE DYNAMIC RANGE vs SUPPLY VOLTAGE

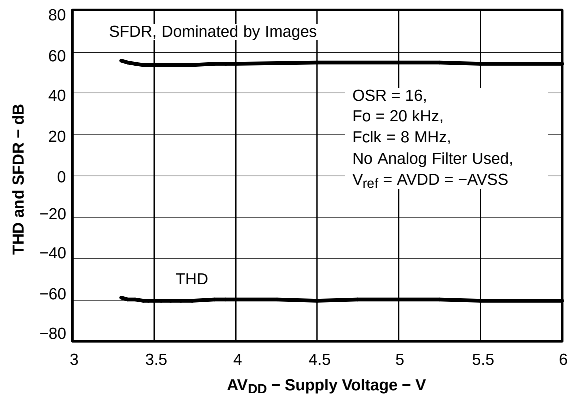


Figure 29.

TOTAL HARMONIC DISTORTION AND SPURIOUS FREE DYNAMIC RANGE vs REFERENCE VOLTAGE

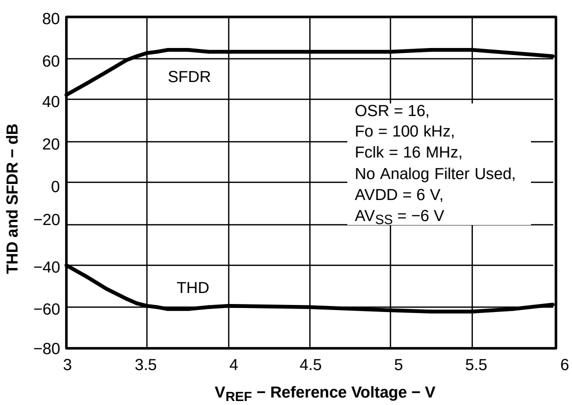


Figure 30.

SOFTWARE-TRIMMED UNIT LINEARITY ERROR vs INPUT CODE

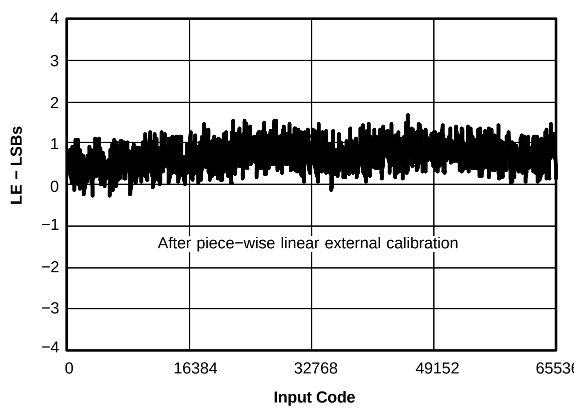


Figure 31.

SOFTWARE-TRIMMED UNIT POWER SPECTRAL DENSITY

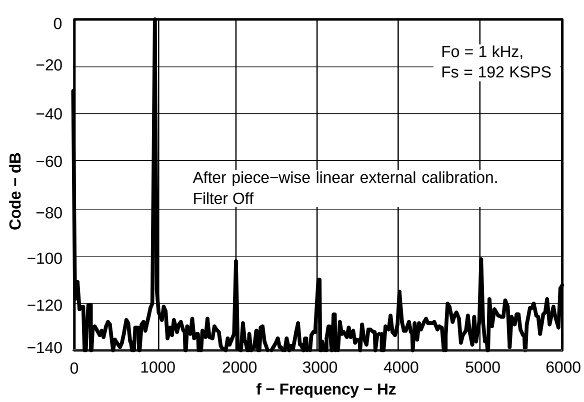


Figure 32.

THEORY OF OPERATION

The traditional high-speed, voltage-output D/A conversion employs a current-output DAC followed by an I-to-V conversion amplifier. For voltage waveform generation applications, these components are typically followed by a sample-and-hold de-glitcher circuit, an analog low-pass filter, and an external buffer to drive low-impedance loads (see Figure 33). Monolithic applications of such traditional architectures suffer from the imperfections of on-chip sample-and-hold circuits, and the analog filters. Multi-chip applications of this traditional architecture suffer from voltage drift problems due to the temperature coefficient mismatches between external passive components and the D/A converter, as well as large circuit size and high cost. DAC8580 is designed to address the problems of traditional high-speed, high-resolution, voltage-output D/A converters.

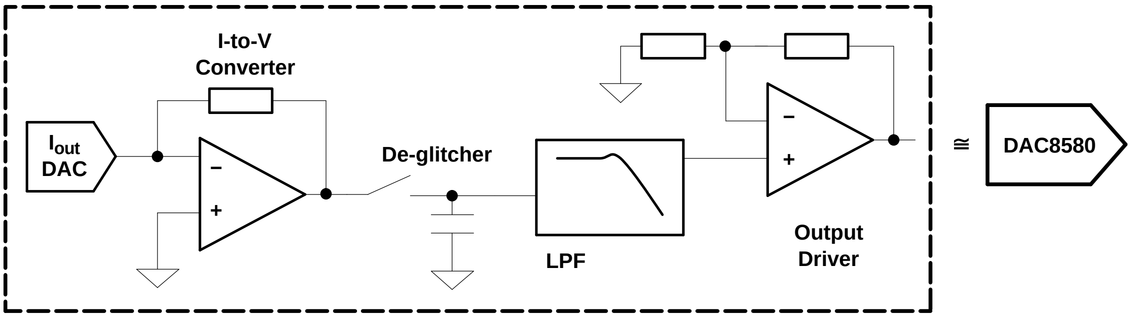


Figure 33. Traditional Voltage Output Waveform Generation Circuitry Replaced by a Single DAC8580

The DAC8580 uses a proprietary, inherently monotonic, high-speed, low-glitch, resistor-string architecture, followed by an on-chip low-noise output amplifier. 16-bit input data is coded in twos-complement format and transmitted using a 3-wire serial interface (MSB first). The input data is sent to an on-chip digital interpolation filter. The filter can be programmed to different oversampling rates, it can be bypassed, or it can be totally disabled. The digital data is then decoded to select a tap voltage of the resistor string. The resistor-string output is sent to a high-speed, low-noise output amplifier. The output buffer has quasi-rail-to-rail swing capability (within 250-mV range of each rail) on a 600-Ω, 200-pF load. Loads of 50 Ω or 75 Ω can also be continuously driven as long as the output current remains within ±25 mA. The DAC8580 reduces the components that are used for implementing sample-and-hold circuits, analog filters, and output driver amplifiers.

The resistor-string DAC architecture provides low glitch, exceptional differential linearity, and temperature stability while the output buffer provides fast settling and exceptionally low noise (20 nV/$\sqrt{Hz}$). The DAC8580 settles well under 1 µs for large signals. The small-signal settling time is less than 150 ns, which enables (oversampled) update rates exceeding 6.7 MSPS. If some small-signal settling error can be tolerated, the DAC8580 can update as fast as 16 MSPS.

Due to the remarkably low glitch energy, the DAC8580 has low harmonic distortion (–70 dB THD for 1-kHz sine wave output). When the linearity error of the DAC8580 is calibrated using a lookup table, the THD performance typically exceeds 98 dBs, without an external S/H circuit.

The DAC8580 needs a low-noise external reference voltage to set its output voltage range. The DAC8580 does not introduce glitches to the external voltage source. This significantly reduces the crosstalk when a single external reference is used to supply the reference voltage for multiple devices.

The DAC8580 has a 3-wire serial interface to communicate with a microprocessor or a DSP. The host is not overloaded by the DAC8580: When the digital filter is on, the host needs only to send 1-out-of-16 data points (for oversampling rate 16). The digital filter of the DAC8580 can generate the remaining data points digitally, on-chip. When the digital filter is disabled (bypassed), the DAC8580 operates as a standard, 16-bit, 2-MSPS, voltage-output DAC. The 1.8-V to 5.5-V digital interface of the DAC8580 enables compatibility with various logic families.

Output Voltage (V_{OUT})

The DAC8580 uses a high-performance rail-to-rail output buffer capable of driving a 600-Ω, 200-pF load with fast 1-µs large-signal settling. The buffer has exceptional noise performance (20 nV/$\sqrt{Hz}$) and fast slew-rate (35 V/µs). The small-signal settling time is under 150 ns, supporting DAC update rates exceeding 6.7 MSPS.

THEORY OF OPERATION (continued)

On power up, a switching circuitry is used to lower power-on transients. Before power up, the DAC output is connected to AGND voltage using a 100-kΩ resistor. During power up, transient output voltages are typically less than 200 mV. Approximately 30 µs after power up, the output gets set to mid-scale value (power-on reset). This mid-scale value is around AGND potential within offset error limits.

Table 1. Two's-Complement Data Format

DAC OUTPUT	DIGITAL CODE	
	BINARY	HEX
+Vref	0111111111111111	7FFF
+Vref/2	0100000000000000	4FFF
0	0000000000000000	0000
–Vref/2	1011111111111111	BFFF
–Vref	1000000000000000	8000

Reference Input Voltage (V_{REF})

The reference input pin VREF is typically tied to a standard 3-V, 4.096-V, or 5-V external reference. Minimum external reference voltage that can be used is 3 V. A 0.1-µF (or less) bypass capacitor is recommended, depending on the load-driving capability of the external voltage reference. To reduce crosstalk and improve settling time, V_{REF} pin is internally buffered by a high-performance amplifier. Pin V_{REF} has a constant 5-kΩ impedance to AGND; therefore, a reference driver should be chosen with care. Because the V_{REF} pin does not induce glitches, multiple DAC8580 devices can share a single external reference without crosstalk concerns. In addition, because the reference pin does not require fast current spikes, the reference voltage generator can be heavily filtered to improve noise performance without hurting settling or distortion. The output range of the DAC8580 is equal to $\pm V_{REF}$. Pin V_{REF} should not be powered before the supply pins. REF3133 and REF3140 are recommended to set the DAC8580 output range to ±3.3 V and ±4.096 V, respectively. The reference bandwidth is 10 MHz (small signal) and 3 MHz (large signal).

Power Supply (AV_{DD}, AV_{SS}, DV_{DD})

The DAC8580 uses ±5-V analog power supplies (AV_{DD}, AV_{SS}) and a 1.8-V to 5.5-V digital supply (DV_{DD}). Analog and digital ground pins (AGND and DGND) are also provided. For low-noise operation, analog and digital power, and ground pins should be separated. Sufficient bypass capacitors, at least 1 µF, should be placed between AV_{DD} and AV_{SS}, AV_{SS} and DGND, and DV_{DD} and DGND pins. Series inductors are not recommended on the supply paths. AV_{DD}, DV_{DD}, AV_{SS}, and V_{REF} should be applied together. V_{REF} must not be applied before AV_{DD} and AV_{SS}. During power up, all digital inputs and the reference input should be kept at zero volts. If any pin is brought high before the power supplies, overvoltage protection circuitry turns on.

SERIAL INTERFACE

The DAC8580 serial interface consists of serial data input pin SDIN, bit clock pin SCLK, and word clock pin FSYNC. The serial interface is designed to support the right-justified (mono) audio format. The serial inputs are 1.8-V to 5.5-V logic compatible.

Data from SDIN pin is continuously clocked into a 16-bit shift register, at each rising edge of SCLK. Falling edge of the FSYNC latches the shift register data into a 16-bit temporary register. The second rising edge of SCLK following the falling edge of FSYNC transfers the data stored in the temporary register to the DAC latch when the digital filter is turned off; when the digital filter is on, data is transferred to the digital filter. That is, DAC data is updated 1.5 clock cycles after the falling edge of FSYNC when the digital filter is off. The shift register continuously performs a shift operation; therefore, on the falling edge of the word clock FSYNC, the last 16 bits received determines the data update (right-justified). Data is received MSB-first. This operation provides a simplified timing for the digital filter, and enables clock rates exceeding 30 MHz. See the timing diagram for details.

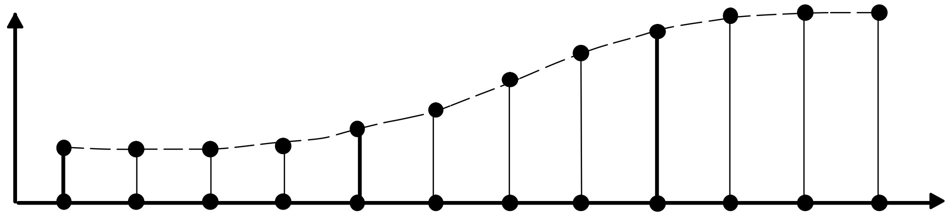
DIGITAL FILTER

The digital filter removes, or simplifies, the component tolerance and temperature drift requirements of the analog filter that follows the DAC8580. Thus, the digital filter reduces the system cost, and improves system reliability. The filter does so at the expense of a 2-input-word delay and some rolloff of the input spectrum, which also is present for the case of an analog filter. The DAC8580 is not a delta-sigma DAC. No noise shaping is performed, and there is no out-of-band noise other than the significantly reduced image frequencies. Driving a 600-Ω load, the DAC8580 idle channel noise typically exceeds 115 dBs over the audio bandwidth.

For output signals exceeding 200 kHz, an analog anti-imaging filter is recommended.

The digital filter is a third-order comb filter with programmable oversampling ratio, which performs a second-order interpolation on the input data.

Figure 34 shows the third-order comb filter effect, which is quadratic interpolation (two-frame delay is not shown).



Data vs time. Third-order comb filtering, quadratic interpolation. Over-sampling ratio = 4.

Figure 34. Data vs Time – Third-Order Comb Filtering

The digital filter has a two-frame delay, independent of the oversampling rate. It does not exactly preserve the input samples. However, it has the nice property of outputting the input sample, if two repetitive input frames are used in a row. It is a finite impulse response (FIR) filter with linear phase, and it does not distort audio phase relationships. The hardware implementation uses feedback; therefore, it is implemented similar to an infinite impulse response (IIR) filter. The number of equivalent FIR coefficients depends on the oversampling rate and is not described in detail. The filter has the following Z-transform and its low-pass frequency response has sinx/x envelope to the third power.

$$H(z) = \left(\frac{1}{N}\,\frac{1 - z^{-N}}{1 - z^{-1}}\right)^3 \qquad (1)$$

The filter serves three major purposes:

The first purpose of the filter is to relax the analog filtering requirement by pushing the image frequencies higher in the spectrum. A single analog RC filter, or no analog filter at all, could work fine. Image frequencies are a fundamental property of an ideal D/A converter, and they can easily dominate the spurious free dynamic range (SFDR) for high-frequency output signals. The digital filter helps remove these image frequencies. Image frequencies appear at the integer multiples of the output data update rate (±) input signal rate. For example, a 1-MSPS DAC generating a 225-kHz sine wave has image frequencies pop up at 775 kHz, 1.225 MHz, 1.775 MHz, 2.25 MHz, etc. The images for the fifth-harmonic are at 112.5 kHz, 887.5 kHz, 1.125 MHz, 1.887 MHz, etc. This 112.5-kHz image for the fifth harmonic pops up even below the 225 kHz fundamental. With an oversampling rate of 16, at 16 MSPS, the image frequency for that same fifth harmonic is pushed back to 16 MHz – 5 × 225 kHz = 14.875 MHz, which can be filtered easily with an RC circuit.

The second purpose of the digital filter is to relax the computational burden on the microcontroller unit driving the DAC8580. At an oversampling rate of 16, the MCU needs to generate only 1-out-of-16 samples; 15 samples out of 16 are computed and generated by the DAC8580 digital filter. Even the input sample itself gets recomputed into a slightly different value by the filter. This way a high-MIPS (million instructions per second) MCU or DSP is not required to drive the DAC8580 for continuous waveform generation applications. A simple microcontroller is sufficient.

The third purpose of the filter is to relax the burden on the DAC8580 output buffer by band limiting the digital input signal. Analog overshoot is not generated during smooth digital signals (filter on). Moreover, when the filter is on, the 150-ns small-signal settling time becomes a dominant factor, as opposed to the 1-µs large-signal settling time. This enables 6.7-MSPS operation with full settling; 16 MSPS is possible if full settling is not necessary. At output update rates above 6.7 MSPS, the user can trade off image frequencies with distortion caused by insufficient settling.

When the filter is bypassed (pin $\overline{\text{BPB}}$ connects to DGND), the DAC latch is loaded directly with the value from the input temporary register. The DAC output changes immediately when the input temporary register is loaded with the new value. If high-speed signals are needed within smooth signals, the filter bypass feature is useful to temporarily switch back to 35 V/µs fast slew rate, while the filter is still in operation.

The DAC8580 uses an infinite impulse response (IIR) implementation of the third-order comb filter. This implementation is stable when there is exactly 16 SCLK rising edges per frame. SCLK should be equally spaced, continuous, and uninterrupted for proper filtered operation. The particular frame during which the $\overline{\text{RSTB}}$ pulse makes a low-to-high transition can contain any number of clock cycles, but after that frame, there must be 16 clocks per frame.

For oversampling ratios of 1, 2, 4, 8, and 16, the DAC8580 analog outputs change every 16, 8, 4, 2, and 1 SCLK rising edges, respectively. For all oversampling ratios, DAC8580 always receives one input data every 16 SCLK cycles. To perform the low-pass function, the digital filter uses the current input, as well as two previous inputs. During power up, when three consecutive inputs are not yet available, the current input and two previous inputs are taken at mid-scale code. The intermediate points between consecutive digital input samples are computed (interpolated) by the digital filter and sent to the output at a higher update rate determined by the oversampling ratio.

The digital filter itself can support update rates up to 16 MSPS due to inherent logic delay limitations. Therefore, the oversampled output update rate of the DAC8580 should not exceed 16 MSPS. For example:

Case 1: Fsclk = 32 MHz
Din = 32 MHz/16 = 2 MSPS
Vout (OSR = 2) = 4 MSPS
Vout (OSR = 4) = 8 MSPS
Vout (OSR = 8) = 16 MSPS
Vout (OSR =16) = Not allowed, limited by the filter update-rate.

Case 2: Fsclk = 16 MHz
Din = 16 MHz/16 = 1 MSPS.
Vout (OSR = 2) = 2 MSPS
Vout (OSR = 4) = 4 MSPS
Vout (OSR = 8) = 8 MSPS
Vout (OSR =16) = 16 MSPS

CONFIGURATION of DIGITAL FILTER

The digital filter is configured through hardware as shown in Table 2.

Table 2. Configuration of Digital Filter

$\overline{\text{BPB}}$	$\overline{\text{RSTB}}$	OSR2	OSR1	$\overline{\text{MUTEB}}$	DESCRIPTION
Don't care	Don't care	Don't care	Don't care	0	OUTPUT CLEAR. The output goes to mid-scale, 1.5 SCLK cycles after falling FSYNC
0	0	Don't care	Don't care	1	STANDARD DAC OPERATION (FILTER OFF) DAC output updates with serial data, 1.5 SCLK after falling FSYNC
1	0	Don't care	Don't care	1	FILTER INITIALIZATION Digital filter gets reset. DAC output goes to mid-scale after receiving SCLK rising edge.
0	1	Don't care	Don't care	1	STANDARD DAC OPERATION (FILTER COMPUTES IN THE BACKGROUND) DAC output updates with serial data, 1.5 SCLK after falling FSYNC
1	1	0	0	1	2X oversampled OPERATION WITH FILTER ON DAC output updates with filtered data, 1.5 SCLK after falling FSYNC and every 8^{th} SCLK thereafter.
1	1	0	1	1	4X oversampled OPERATION WITH FILTER ON DAC output updates with filtered data, 1.5 SCLK after falling FSYNC and every 4^{th} SCLK thereafter.
1	1	1	0	1	8X oversampled OPERATION WITH FILTER ON DAC output updates with filter data, 1.5 SCLK after falling FSYNC and every 2^{nd} SCLK thereafter.
1	1	1	1	1	16X oversampled OPERATION WITH FILTER ON DAC output updates with filter data, 1.5 SCLK after falling FSYNC and every SCLK thereafter.

Mute Function (Pin $\overline{\text{MUTEB}}$)

Mute function is implemented by setting the DAC output voltage to mid-scale (~0 V). The $\overline{\text{MUTEB}}$ pin is active low, and is synchronized with the frame. That is, the DAC latch and DAC output are immediately set to mid-scale during the first update while the $\overline{\text{MUTEB}}$ pin is low. The $\overline{\text{MUTEB}}$ pin works independent of the serial data transfer, or the digital filter. Neither the serial input, nor the digital filter data get interrupted or get lost while the output is set at mid-scale with $\overline{\text{MUTEB}}$. The first DAC update occurring after the $\overline{\text{MUTEB}}$ pin goes high sets the DAC latch and DAC output to the next desired value. $\overline{\text{MUTEB}}$ pin must be kept at logic low level before power up.

Oversampling Rate (Pin OSR2, OSR1)

oversampling rate of the digital filter is set via pins OSR2 and OSR1.

OSR2	OSR1	OVERSAMPLING RATE
0	0	2
0	1	4
1	0	8
1	1	16

The DAC8580 can support these oversampling ratios as long as the oversampled update rate does not exceed 16 MSPS. The oversampling ratio should be set at power up. OSR1 and OSR2 pins must be kept at logic-low level before power up.

Digital Filter Bypass (Pin $\overline{\text{BPB}}$)

The digital filter can be asynchronously bypassed via pin $\overline{\text{BPB}}$. When pin $\overline{\text{BPB}}$ is active low, the digital filter is bypassed. In this case, the DAC latch receives the data from the temporary register, not from the digital filter. When the series input data is latched into the temporary register from the input shift register, the DAC latch and DAC output are updated immediately with the new value of the temporary register. When pin $\overline{\text{BPB}}$ is high, digital filter is not bypassed. The DAC latch is loaded with the output of the digital filter, not with the content of the temporary register. The digital filter generates the data and transfers it to the DAC latch.

When the digital filter is bypassed, the filter keeps running. A bypass does not disrupt the internal computations of the digital filter. When the $\overline{\text{BPB}}$ pin goes high, the oversampled operation resumes without any discontinuity of the filtered output. The $\overline{BPB}$ pin multiplexes the DAC input between the filter output and the output of the temporary register. Certain applications require generation of smooth waveforms, combined with fast edges. A good example is the CRT positioning signal, where a smooth ramp is followed by a fast blanking pulse. The digital low-pass filter offers the capability to generate smooth ramp waveforms (with filter on) and fast blanking pulse (with filter bypassed). The bypass feature offers on-the-fly capability to switch between smooth filtered operation and high-speed unfiltered operation. The $\overline{BPB}$ pin must be kept at logic low before power up.

Digital Filter Asynchronous Reset (Pin $\overline{RSTB}$)

The digital filter equation is invalidated if other than 16 clocks per frame are received. This condition causes numerical instability; the $\overline{RSTB}$ pin is used for recovering from such errors without forcing the user to issue a power-on reset. The $\overline{RSTB}$ digital input is an active-low, asynchronous filter reset. The $\overline{RSTB}$ does not reset the serial interface. Immediately after $\overline{RSTB}$ becomes low, all filter registers were cleared, all filter clocks are stopped, all digital filter switching activities are stopped in order to lower switching noise and digital power consumption. If the digital filter is not needed, the $\overline{RSTB}$ and $\overline{BPB}$ pins should both be tied to a logic zero. The filter reset operation always occurs asynchronously when $\overline{RSTB}$ = 0. However, the effect of $\overline{RSTB}$ = 0 at the DAC output (Vout ~ 0 V) cannot be observed if the SCLK is stopped, or if $\overline{BPB}$ = 0. Pin $\overline{RSTB}$ must be kept at logic low before power up.

The DAC8580 monitors for receipt of 16 clocks per frame and issues an automatic filter reset if other than 16 clocks per frame is received. This auto-reset is synchronized with the FSYNC line.

$\overline{RSTB}$	$\overline{BPB}$	OPERATION
0	0	Conventional DAC operation: Shutdown and disconnect the digital filter
0	1	Filter reset. DAC output becomes ~0 V only if SCLK is continuously running.
1	0	Filter bypass. Conventional DAC operation resumes, while filter is on.
1	1	Filtered operation. DAC outputs filtered data at the oversampling rate.

APPLICATION INFORMATION

CRT Projection TV Digital Convergence

The DAC8580 is an ideal component for the digital convergence units of the three-tube projection TV sets. Digital convergence applications require the generation of precision voltage waveforms with approximately 150-kHz bandwidth. Six DAC8580s are needed for one TV set to generate convergence waveforms for horizontal and vertical red, green, and blue, as seen in Figure 35. A single external reference, REF3025, can support all six DACs. The low temperature drift, low glitch, and low noise of the DAC8580 improve the picture quality and color drift.

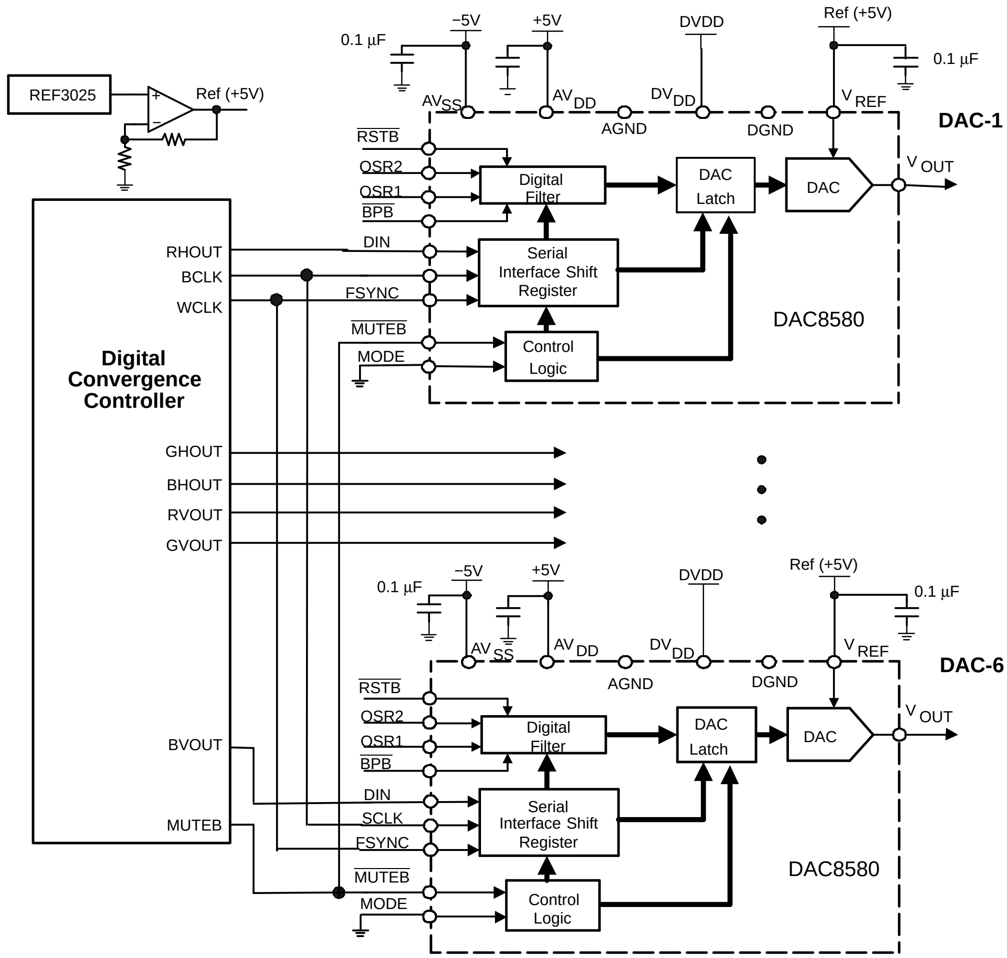


Figure 35. DAC8580 for Projection TV Digital Convergence

PACKAGE OPTION ADDENDUM

27-Sep-2005

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC8580IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8580IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8580IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8580IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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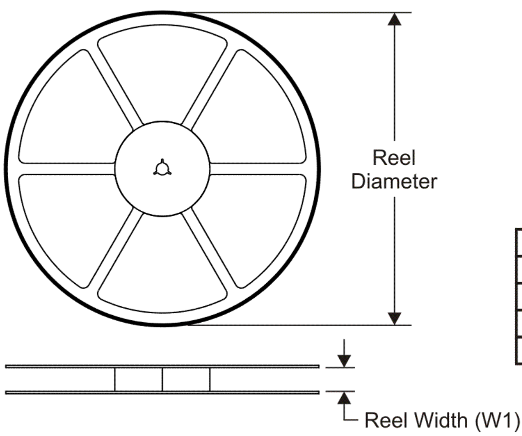
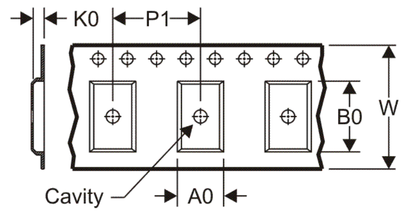
TAPE AND REEL INFORMATION

REEL DIMENSIONS

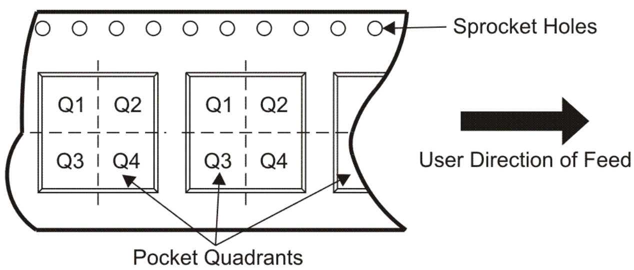


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

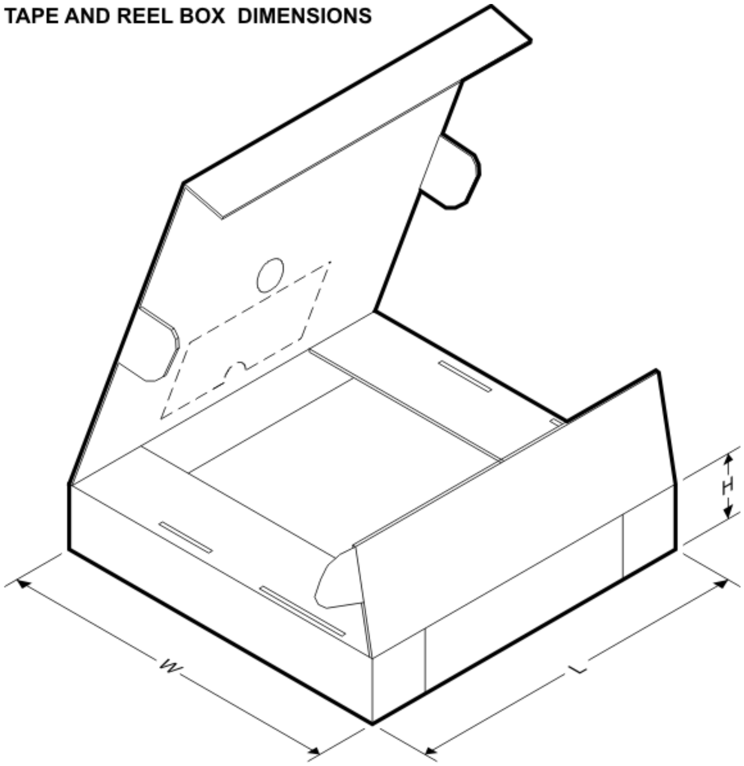
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8580IPWR	TSSOP	PW	16	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

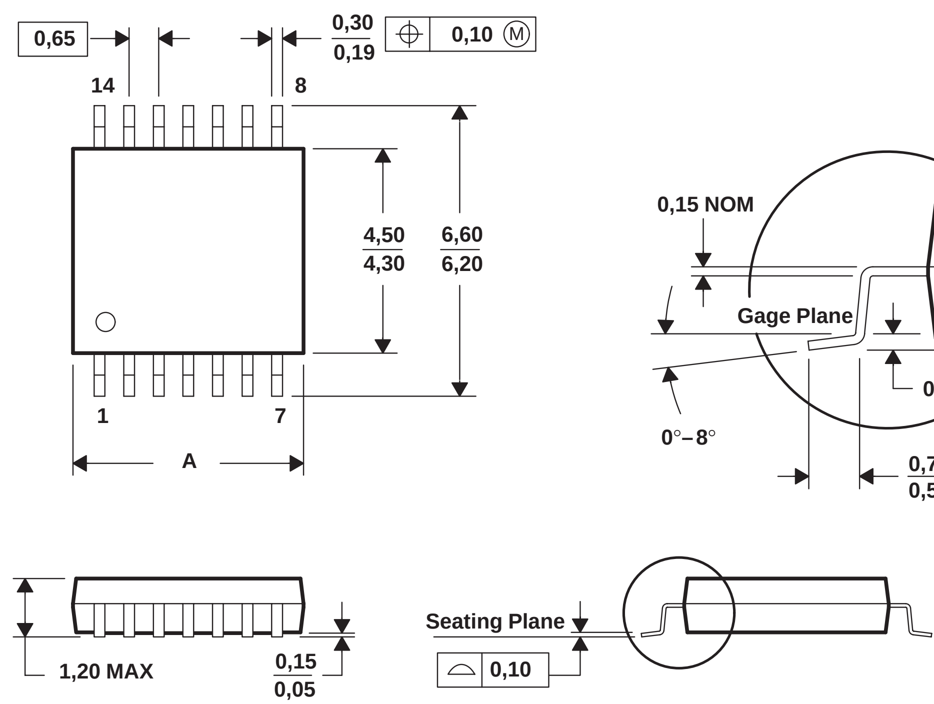


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8580IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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